ANNOUNCING AN INTENSIVE HALF-DAY TUTORIAL ON

THE NEXT GENERATION OF ELECTRONIC PARTS: PROCESSES, TESTS, APPLICATIONS AND RISKS

August 24, 1999 at the Radisson Hotel Berkeley Marina, Berkeley, CA

Presented By

Professor Michael Pecht
University of Maryland

Historically, Plastic Encapsulated Microcircuits (PEMs) have been used in commercial and telecommunications electronics and consequently have had a large manufacturing base. With major advantages in cost, size, weight, performance, and availability, plastic packages have attracted 97% of the market share of worldwide microcircuit sales, although they encountered formidable challenges in gaining acceptance for use in government and military applications. In fact, it was only in the early 1990s that the industry dispelled the notion that hermetic packages were superior in reliability to plastic packages, in spite of their low production and procurement volumes and the outdated government and defense department standards and handbooks associated with their manufacture and use.

Today, high-quality, high-reliability, high-performance, and low-cost plastic-encapsulated microcircuits are common. The question is now, what's on the horizon? Thanks to new packaging materials, improved device architectures, increased design for reliability and other important developments, new types of packaged devices are becoming dominant in the computer, commercial and telecommunications market. Like previous parts, these parts will require special care in their selection, quality assessment, assembly reliability in the targeted aerospace,industial and military applications and determination of life cycle risk.

COURSE OUTLINE

The course is divided into two sections; the first describing the state-of-the-industry and the second describing the issues

which must be addressed to select and implement the next generation of electronic parts. Each section presents the concepts, theory & practice, with principles illustrated with examples.

SECTION 1. THE CHANGING WORLD

A presentation of the development of microcircuits and the technical innovations, and economic and political conditions, that drive the developments. Device and packaging technologies are compared in terms of their strengths and weaknesses (both technical and economic).

- Device and package classification
- Device and package construction and fabrication
- Worldwide market trends
- Technology trends
- Reliability trends
- Potential opportunities
- Hurdles to insertion

SECTION 2. SELECTING THE RIGHT PART-AN EXERCISE IN RISK ASSESSMENT

A comprehensive, pro-active process for specifying, procuring, and managing the use of electronic components in design, manufacturing and in-service is essential for success. This session presents the process and covers areas that must be implemented, and the methods necessary to apply the next generation of electronic devices and packages.

- System level requirements and constraints
- Technology sensing
- Manufacturer and manufacturer parts quality and integrity assessment
- Distributor assessment
- Application-specific reliability assessment
- Performance of parts within the application
- Life cycle mismatch assessment
- Assembly assessment
- Parts and product management

The Registration Fee for this intensive half-day tutorial (1:00-5:30 pm) is $425.00 inclusive of lunch & afternoon break. Attendees will receive a complete handout of the course

presentation. Registration Fee received after August 9 will be $500.00.

*THIS TUTORIAL IS IN CONJUCTION WITH THE **1999 MILITARY/AEROSPACE (TRANSPORTATION) COTS CONFERENCE**, being held AUGUST 25-27 AT THE SAME LOCATION.*

ABOUT THE INSTRUCTOR

Michael Pecht is the Director of the CALCE Electronic Products and Systems Consortium (EPSC) at the University of Maryland and a Full Professor. Dr. Pecht has a BS in Acoustics, a MS in Electrical Engineering and a MS and PhD in Engineering Mechanics from the University of Wisconsin. He is a Professional Engineer, an IEEE Fellow, an ASME Fellow and a Westinghouse Fellow. He has written eleven books on electronics products development. He served as chief editor of the IEEE Transactions on Reliability for eight years and on the advisory board of IEEE Spectrum. He is currently the chief editor for Microelectronics Reliability International. He serves on the board of advisors for various companies and provides expertise in design, test and reliability assessment of electronics products and systems.

TUTORIAL REGISTRATION

Registration Fee for the tutorial is $425.00, which includes lunch, PM break and complete lecture notes. Registration Fee after August 9 will be $500.00

Name .....

Organization .....

Address .....

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Zip/Post Code ..... **Country** .....

Tel: ..... **Fax:** .....

Email: .....

Make checks payable to THE C3I, Inc. Any international attendees paying by check must have the check drawn from a US bank and include any additional processing fees. Credit Cards NOT Accepted. Send checks to:

THE C3I, Inc.
Attention: Edward B. Hakim
2412 Emerson Avenue
Spring Lake, NJ 07762
Tele or Fax: 732-449-4729 Email: ebhakim@bellatlantic.net

TRANSPORTATION OPTIONS
TO THE

RADISSON

HOTEL BERKELEY MARINA

200 Marina Boulevard, Berkeley, California 94710

SHUTTLE COMPANIES
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Reservations Required - Hotel Guests may call Guest Services for assistance in Making your Reservations.
24 Hours Advance Notice is recommended.

BAYPORTER EXPRESS 415 – 467 -1800
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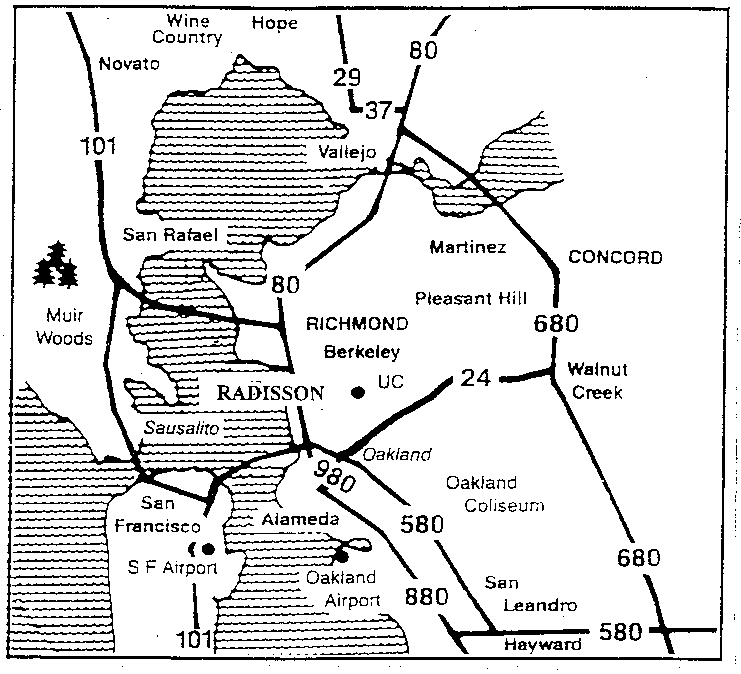

DIRECTIONS TO ↑ ↓

Radisson Hotel Berkeley Marina

From San Francisco:

Take **101 North** to **I-80 East** staying left once over and across the Bay Bridge . Exit at University Ave. Make a U -Turn at the first traffic light (6th St.) You will be heading West toward the Bay on University. Make **a right on Marina Blvd.**
Hotel entrance is about one quarter of a mile ahead on your left.

From Oakland:

Take **Hwy 880 North** to **Hwy 580 West** toward San Francisco, then **to 80 East Berkeley. Exit at University Ave.** Make a U -Turn at the first traffic light (6th St.) You will be heading West toward the Bay on University. Make **a right on Marina Blvd.**
Hotel entrance is about one quarter of a mile ahead on your left.

From Sacramento:

Take 1- **80 South** to Berkeley. **Exit at University Ave.** Make the first **left at the stop sign** after looping around the exit ramp onto University Ave. Make a right onto Marina Blvd. Hotel entrance is about one quarter of a mile ahead on your left.